**SARASWATI MAHILA MAHAVIDHYALAYA, PALWAL**

**LESSON-PLAN**

**Class: BSC (CS) IST YEAR Semester: ODD**

**Subject:** **Computer Architecture Session: 2020-21**

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| **Lecture Number** | **TOPIC** |
|  | **UNIT 1** |
| **L 1-20** | OR, AND, NOT, XOR Gates. |
| De Morgan’s theorem. |
| Laws and theorem of Boolean algebra. |
| Simplifying logic circuits—sum of product and product of sum form. |
| Continue. |
| Continue. |
| Continue. |
| Algebraic simplification. |
| Continue. |
| Karnaugh simplification. |
| Continue. |
| Continue. |
| Continue. |
| Continue. |
| CLASS TEST. |
|  | **UNIT 2** |
| **L 21-35** | Arithmetic Circuits: Adder, Subtractor. |
| Parallel Binary-adder/Sub tractor. |
| Binary Multiplier and Divider. |
| Continue. |
| Combinational Circuits: Decoders and Encoder. |
| Continue. |
| Multiplexer and De-multiplexer circuits. |
| Continue. |
| Design of code Converters. |
| Continue. |
| CLASS TEST |
|  | **UNIT 3** |
| **L 36-55** | Introduction of Sequential Circuits. |
| Flip-flop-S-R. |
| Continue. |
| D, J-K, T Flip Flops. |
| Continue. |
| Clocked Flip-flop. |
| Race Around condition, Master-Slave Flip-Flop. |
| Realization of One Flip-Flop using other Flip-Flop. |
| Continue. |
| Continue. |
| Shift-Registers. |
| Counters-Ripple. |
| Modular Synchronous. |
| Ring & Twisted-Ring Counter. |
| Continue. |
| CLASS TEST |
|  | **UNIT 4** |
| **L 56-70** | Register transfer Language. |
| Bus and Memory Transfer. |
| Continue. |
| Arithmetic Micro-operations. |
| Logic Micro-operations. |
| Shift Micro-operations. |
| Continue. |
| Instruction and instructions codes. |
| computer instructions. |
| timing and control. |
| instruction cycle. |
| memory references instructions. |
| Continue. |
| input- output reference instructions and interrupts. |
| Continue. |
| CLASS TEST |

**SONIYA RANI**

**Asst Prof. in CS**